REMARKS

Reconsideration of the present application is respectfully requested.

Summary of Office Action

Claims 44, 45, 49, 50 and 63 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Claims 44, 45, 49, 50 and 63 stand rejected under 35 U.S.C. § 103(a) based on U.S. Patent no. 4,766,566 of Chuang ("Chuang") in view of U.S. Patent no. 5,313,331 of Labrousse et al. ("Labrousse"), in view of U.S. Patent no. 4,766,566 of Yokouchi ("Yokouchi"), in view of U.S. Patent no. 4,346,437 of Blahut et al ("Blahut").

Summary of Amendments

Claims 1-43, 38 and 51-62 were previously canceled. In this amendment, claims 44, 49 and 63 have been amended. Claim 50 has been canceled. No new matter has been added.

Discussion of Rejections

Section 112(1) Rejections

The Examiner states, "The limitation from claims 44 and 63 'A second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units' is not contained within the specification upon a cursory glance." (Office Action, p. 2). Applicant identified support for these limitations on page 8 of

Applicant's response filed on 5/17/2007 (i.e., referring to paragraphs [0044] – [0046], especially in Table 1, of Applicant's substitute specification).

In response to Applicant's response, the Examiner states (Office Action, page 9):

> [T]here isn't any mention that information stating where an operand is coming from is necessarily encoded within the instructions in table 1. The examiner believes that this could also be a list of options where the register values could be bypassed from. If the applicant has further evidence that the operand sources must be encoded within the instruction itself, then the examiner would be convinced the limitation has written description support and would withdraw the rejection.

Applicant again respectfully submits that the previously identified paragraphs and Table 1 of the substitute specification clearly support for the limitations in question. The Examiner's reluctance to agree on this issue is not understood (also, the Examiner's statement, ". . . could also be a list of options where the register values can be bypassed from" is not entirely clear to Applicant). Applicant respectfully draws the Examiner's attention to the first sentence of paragraph [0046] of the substitute specification, which states, "As an example of the free pipeline assembly code level, ALU instructions include those listed in the following table" (referring to table 1)(emphasis added). Hence, table 1 itself clearly gives examples of the instructions in question, and those instructions clearly reference individual outputs of functional units, R and S. As previously mentioned, the note immediately following table 1 expressly states that operands R and S each can be selected from the various different buses, A (register), D (data-memory), M (multipler) and Q (barrel-shfter). Furthermore, when read in conjunction with the rest of the description, particularly Figure 3 and its associated text, there would be absolutely no doubt in the mind of a person of ordinary skill in the art that what is being described includes an assembly code level (the "free

pipeline" level) which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units.

Therefore, Applicant again respectfully submits that the rejection under section 112 is improper and requests that it be withdrawn.

Prior Art Rejections

Claim 44 as amended recites:

44. (Currently amended) A processor comprising:
at least three functional units coupled to each other to execute operations defined from an instruction set of the processor, the at least three functional units including an arithmetic logic unit (ALU) and a multiplier, the instruction set having a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor, the hierarchy of instruction levels including
a RISC/CISC assembly code level,
a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units, and
a vector processing assembly code level, using which an individual instruction can be used to cause an operation to be automatically repeated sequentially a programmable number of times on different data words;
a plurality of control registers, the plurality of hierarchical instruction levels further comprising a fourth level corresponding to the control registers, using which individual instruction words executed by one or more of the functional units can be extended by bits in the control registers on a per-instruction-cycle basis; and
a bus routing structure that includes **at least three dedicated output buses, including a separate dedicated output bus for each of the at least three functional units, each of the at least three dedicated output buses being dedicated to convey data output by a separate one of the at least three functional units, each of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses**. (Emphasis added.)

The cited references failed to disclose such a processor, particularly one which includes a bus routing structure that includes at least three dedicated output buses, including a separate dedicated output bus for each of the at least three functional units, each of the at least three dedicated output buses being dedicated to convey data output by a separate one of the at least three functional units, each of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses.

Regarding the above-emphasized limitations, the Examiner appears to rely upon Chuang as disclosing similar limitations in rejecting dependent claims 49 and 50. The Examiner cites Chuang at Figure 7, elements 63 and 68, and col. 10, lines 18-41, stating "each functionality and it has an output bus to the data on," and "[t]he output registers are coupled to the functioning units and the output buses. Thus having the same functionality." (Office Action, p. 8).

Applicant respectfully submits that Chuang fails to disclose or suggest anything similar to those claims or the above emphasized claim limitations. Assuming *arguendo* the outputs of the various units in Chuang's Fig. 7 (e.g., multiplier 63, output register 68, etc.) can be considered dedicated output "buses" of functional units, Applicant finds no disclosure in Chuang that each of those (at least three) units has an input coupled directly to one of those dedicated output buses (it may help the Examiner to visualize the difference by comparing Chuang's Fig. 7 to Applicant's Figure 3, however, Applicant believes the added claim language clearly captures a fundamental difference without any need for clarification). If the Examiner still disagrees and intends to maintain this

rejection, the Examiner is requested to be more specific in the next Office Action about exactly which signal lines in Chuang are considered to be the dedicated output buses of claims 44 and 63, which elements in Chuang are considered to be the at least three functional units, and how each of them have an input coupled directly to one of those dedicated output buses.

Furthermore, Applicant respectfully submits that the Examiner's statement, "Thus having the same functionality" (office action, page 8) is inapposite, because the limitations in question recite specific structural interconnections. Hence, the mere disclosure of equivalent or even identical function does not by itself satisfy these claim limitations.

For at least the above reasons, therefore, no combination of the cited references discloses or suggest *all of the limitations* of claim 44 or claim 63. Furthermore, there would there would be no reason for one of ordinary skill they are to try to combine the cited references in the manner alleged, to achieve the present invention is claimed. Therefore, claims 44 and 63 and any claims which depend on them are patentable over the cited art.

Dependent Claims

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicants' silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

Conclusion

For the foregoing reasons, the present application is believed to be in condition for allowance, and such action is earnestly requested.

If any additional fee is required, please charge Deposit Account No. 02-2666.

Respectfully submitted,
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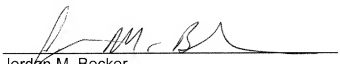

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